

Abstract of the Disclosure:

A dynamic RAM semiconductor memory with a shared sense amplifier organization concept, in which the cell arrays are subdivided into blocks whose bit lines are connected in pairs
5 from two adjacent blocks in each case to a common sense amplifier and the sense amplifiers are disposed between the cell blocks. In which case bit line switches are disposed in sense amplifier strips - lying between the blocks - between in each case two adjacent sense amplifiers in order to
10 momentarily connect the other ends - not connected to the sense amplifiers - of two bit line pairs from the adjacent cell blocks during a precharge phase of a bit line pair activated directly beforehand. The precharge phase takes place at the start of a charge equalization phase.

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